## AMENDMENTS TO THE CLAIMS

- 1. (Cancelled)
- 2. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is an NMOS device, then applying includes: providing a slightly negative voltage from the memory cell to the gate of the transistor.
- 3. (Original) The method of Claim 2, wherein the slightly negative voltage is between 0 and approximately –0.2 V.
- 4. (Original) The method of Claim 2, wherein the slightly negative voltage is approximately –0.1 V.
- 5. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising: storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is an NMOS device, then applying includes: providing a first voltage from the memory cell to the gate of the transistor, wherein the first voltage is slightly less than a second voltage provided to a source of the transistor.

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between 0 and approximately 0.2 V.

6. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is an NMOS device having a gate voltage of 0 V, then applying includes:

(Original) The method of Claim 6, wherein the slightly positive voltage is

providing a slightly positive voltage to a source of the transistor.

- 8. (Original) The method of Claim 6, wherein the slightly positive voltage is approximately 0.1 V.
- 9. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is an NMOS device, then applying includes: providing a first voltage to a source of the transistor, wherein the first voltage is slightly greater than a second voltage provided from the memory cell to the gate of the transistor.
- 10. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed.

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wherein if the transistor is a PMOS device having a source voltage of VDD, then applying includes:

providing a slightly more positive voltage than VDD from the memory cell to the gate of the transistor.

- 11. (Original) The method of Claim 10, wherein the slightly more positive voltage is VDD + N, wherein  $0 < N \le 0.2 V$ .
- 12. (Original) The method of Claim 10, wherein the slightly negative voltage is approximately VDD + 0.1 V.
- 13. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is a PMOS device, then applying includes: providing a first voltage from the memory cell to the gate of the transistor, wherein the first voltage is slightly greater than a second voltage provided to a source of the transistor.
- 14. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is a PMOS device having a gate voltage of VDD, then applying includes:

providing a slightly less positive voltage than VDD to a source of the transistor.

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- 15. (Original) The method of Claim 14, wherein the slightly less positive voltage is VDD N, wherein  $0 < N \le 0.2 V$ .
- 16. (Original) The method of Claim 14, wherein the slightly positive voltage is approximately VDD 0.1 V.
- 17. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein if the transistor is a PMOS device, then applying includes: providing a first voltage to a source of the transistor, wherein the first voltage is slightly less than a second voltage provided from the memory cell to the gate of the transistor.
- 18. (Currently Amended) The method of Claim 1, A method of suppressing subthreshold leakage in a transistor of an integrated circuit, the method comprising:

  storing a value in a memory cell coupled to a gate of the transistor; and applying a gate to source voltage to the transistor that under-drives the transistor, wherein the sub-threshold leakage in the transistor is suppressed, wherein applying includes:

providing a level shifter that receives a logic signal from the integrated circuit and generates a modified gate voltage for the transistor,

wherein the modified gate voltage is one of:

slightly less than a source voltage of the transistor, if the transistor is an NMOS device, and

slightly greater than a source voltage of the transistor, if the transistor is a PMOS device.

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19. (Currently Amended) A memory cell for suppressing sub-threshold leakage in a transistor, the memory cell comprising:

a plurality of transistors configurable to store a value,
wherein the value can under-drive the transistor in its off state, [[and]]
wherein under-driving the transistor suppresses the sub-threshold leakage in
the transistor,

wherein if the transistor is an NMOS device having a source voltage of VSS and the memory cell drives a gate of the transistor, then the value is slightly more negative than VSS;

wherein if the transistor is a PMOS device having a source voltage of VDD and the memory cell drives a gate of the transistor, then the value is slightly more positive than VDD;

wherein if the transistor is an NMOS device having a gate voltage of VSS and the memory cell drives a source of the transistor, then the value is slightly more positive than VSS; and

wherein if the transistor is a PMOS device having a gate voltage of VDD and the memory cell drives a source of the transistor, then the value is slightly less than VDD.

Claims 20 - 25. (Cancelled)